Remarks:

The correct deletions have been added to claim 9, as requested. The remaining original underlinings and deletions have been retained for ease of reference.

For completeness, applicant reiterates the Remarks made in the original Response.

The examiner and supervisor are thanked for the interview.

The s112 objections and s103 rejections were discussed. Applicant clarified and distinguished the present invention. In particular:

35 USC 112

The Office action states that it was unclear how a gate could form a node on one side of itself. It is respectfully pointed out that claim 2 does not define the gate as forming a node. Instead, claim 2 states that there is a high voltage node on one side of the gate and a low voltage node on the other side of the gate.

The Office action also states that it is unclear how the gate can be formed in the n-well. Again it is respectfully pointed out that claim 2 does not state that there is a gate in the n-well . It simply states that the LVTSCR includes a gate. There is a comma after the word "gate". It is the first n+ region and the first p+ region that are formed in the n-well according to claim 2.

The Office Action states that it was unclear as to which element is the p-type element. Claim 2 refers to a p-n junction and mentions an n-type material as defined by the additional n+ region. The p-type material that abuts this n+ region is the p-well and therefore the p-n junction is between the p-well and the additional n+ region. The reason why the second p+ region is mentioned is that the p-well needs a p+ region to define a diode contact. Claim 2 has been amended to clarify this point.

Claim 3 was said to be unclear whether "said at least one diode" was the same diode as mentioned earlier in the claim. The use of the word "said" is standard claim language terminology to explicitly refer to the previously cited element. Since there is no other diode or set of diodes it has to refer to the earlier mentioned diode or set of diodes.

Regarding claim 4 the Office action states that it is unclear how a current path can be lower than a p-well. It is respectfully pointed out that the current path is not lower. Instead the resistance of the current path is lower since it includes the diodes.

The Office action states that it is unclear between which elements the p-n regions are formed and whether the additional n+ regions and additional p+ regions are the same as those mentioned in claim 2. Claim 2 had mentioned at least one additional n+ region but no additional p+ regions. Claim 9 introduces multiple diodes by adding more additional n+ regions and introduces additional p+ regions thereby providing a first diode between one additional n+ region and p-well (with the second p+ region forming the contact for this first diode) and provides for further diodes by providing additional pairs of additional n+ regions and additional p+ regions as illustrated in Figure 4. Claim 9 has been further amended to clarify the concept of multiple diodes in the p-well.

35 USC 103

After pointing out the first n+ and first p+ regions in the n-well, and the second n+ and second p+ regions in the p-well it was agreed at the interview that Ker did not teach an additional n+ region in the p-well and therefore was not a s102 reference.

As discussed in the previous response, Figure 8 of Ker simply provides the typical LVTSCR structure with first n+ and p+ regions 214, 212 in the n-well and second n+ and p+ regions 220, 222 in the p-well. The regions 220 and 222 are thus standard regions in an LVTSCR and correspond to the second n+ and second p+ region mentioned in the claim.
Ker does not teach or suggest providing an additional n+ region in the p-well, over and above the second n+ and second p+ regions of the standard LVTSCR.

The applicant then considered the argument in the Office action that Ker in Figure 10B teaches the use of diodes 324 which provides the motivation for adding diodes internally as in the present invention.

However, by adding the diodes internally between anode and cathode of the LVTSCR of the present invention, the voltage difference over the LVTSCR of the present invention does not change but instead the internal diodes provide a low resistance internal current path which causes a higher current through the device during an ESD event and has the effect of increasing the holding voltage.

In contrast, the external diodes shown in Ker are provided not between anode and cathode of the SCR device but between cathode and Vss. This cause an external voltage drop over the diodes between the cathode and Vss, which leaves a lower voltage difference over the device between anode and cathode because part of the voltage difference between Vdd and Vss is dropped across the diodes. The internal resistance of the Ker SCR device is not changed, however, which means that the lower voltage over the device will cause a lower current through the device. Thus the present invention teaches the opposite to Ker and therefore Ker teaches away from the present invention.

It cannot therefore be said that it would be obvious to provide internal diodes in Ker because that would cause the opposite effect to what Ker is trying to achieve.

Functionally, Ker deals with an entirely different problem, namely the reduction in triggering voltage (the voltage for causing the SCR device to go into double avalanche conduction), whereas the present invention deals with increasing the holding voltage to avoid latch-up (the voltage at which the SCR device will stop conducting after an ESD event).

Thus, since the addition of internal diodes to Ker would teach away from the Ker invention, it would not be obvious to combine Ker with Yu or any other teachings that show internal diodes. Also Yu fails to teach an LVTSCR with internal forwardly biased diodes. Thus Ker and Yu on their own do not teach the present invention. Also, as discussed above, Yu cannot be combined with Ker since the resultant structure would teach away from what Ker is seeking to achieve.

It was agreed that the examiner would review the arguments in the present response and make a final decision at that time. If at that time he still believes that it would be obvious to provide internal diodes to the structure of Ker even though it would teach away from the intention of Ker by increasing the current rather than decreasing the current through the device, applicant would

be given the opportunity to file a pre-appeal brief to have the matter reviewed by to supervising examiners.

Applicant thanks the examiner and his supervisor for the telephone interview and requests that the claims be allowed since they are structurally different from Ker and Yu, and because they fail to teach or suggest an LVTSCR with internal forward biased diodes in the p-well of the diode. Also Ker and Yu are functionally different since neither teaches or suggests a new approach to increasing holding voltage of an SCR device by forming an internal low resistance current path.

Respectfully Submitted,

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